**Logic Design Laboratory**

**CSC206A**

**B.Tech. III Semester**

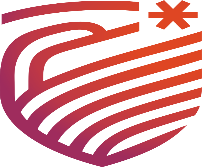
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**Department: Computer Science and**

**Engineering**

**Faculty of Engineering & Technology**

**Ramaiah University of Applied Sciences**



**Ramaiah University of Applied Sciences**

Private University Established in Karnataka State by Act No. 15 of 2013

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| --- | --- |
| Faculty | Engineering & Technology |
| Programme | B. Tech. in Computer Science and engineering |
| Year/Semester | 3rd Semester |
| Name of the Laboratory | Logic Design Laboratory |
| Laboratory Code | CSC206A |

List of Experiments

**Day-1**

1. Build digital circuits using logic gates. Verify using truth table.

W=BC+~BC

X=~AB+~AB~C+~ABCD+~AB~C~DE

Y=BD+B(D+~E)+~D(D+F)

Z=A~BC+~ABC+~A~BC

AB+A(B+C)+B(B+C)

(A~B(C+BD)+~A~B)C

~A~B~C+~ABC+A~B~C+A~BC+ABC

(A+~A)(AB+ AB~C)

X~Y~Z+~XYZ

**Day-2**

1. Build a circuit which is dual of the given expression. Verify using truth table.

~(~(AB)~(CD))=AB+CD

~(~(AB)C)=AB+~C

~(A~(BC))=~A+BC

~(ABC)=~A+~B+~C

A(~(B+C)=A~B~C

~(~AB(C+~D)+E)=A~E+~B~E+~CD~E

# Laboratory 1

Title of the Laboratory Exercise

Introduction and Purpose of Experiment

**In this laboratory exercises students get familiar with Logisim.**

**Build digital circuits using logic gates. Verify using truth table.**

1. Aim and Objectives

Aim

* To use Logisim

1. Objectives

At the end of this lab, the student will be able to

* Explain the features and use of Logisim
* Design digital circuits using Logisim

1. Experimental Procedure

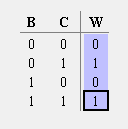
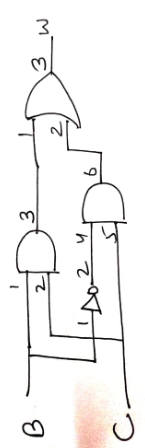
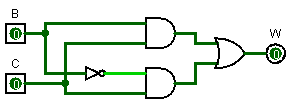
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| Aim and objective |
| Requirement and equipment used |
| Simulation and realization |
| Verification results and Analysis |
| Conclusion |
| Limitations and Recommendations |
| Viva |

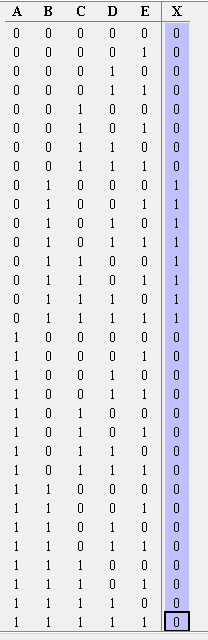
Students are given a set of logical expression. Using Logisim students are expected to build circuit. And test.

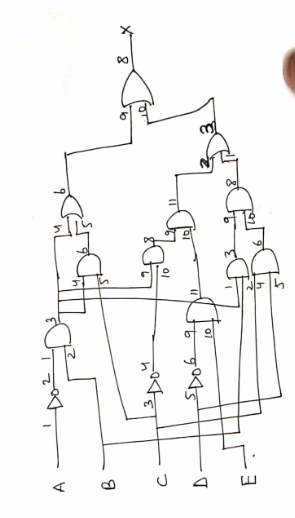
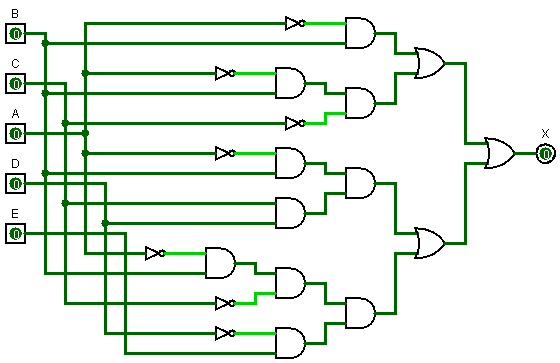
1. Questions
   1. **W=BC+~BC**
   2. **X=~AB+~AB~C+~ABCD+~AB~C~DE**
   3. **Y=BD+B(D+~E)+~D(D+F)**
   4. **Z=A~BC+~ABC+~A~BC**
   5. **AB+A(B+C)+B(B+C)**
   6. **(A~B(C+BD)+~A~B)C**
   7. **~A~B~C+~ABC+A~B~C+A~BC+ABC**
   8. **(A+~A)(AB+ AB~C)**
   9. **X~Y~Z+~XYZ**

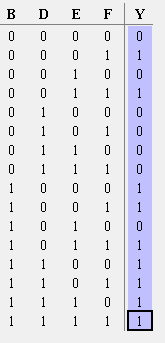
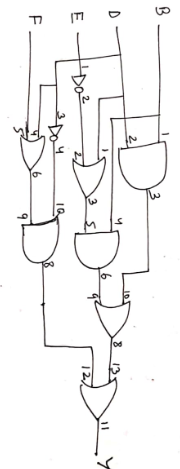
## **Solutions:**

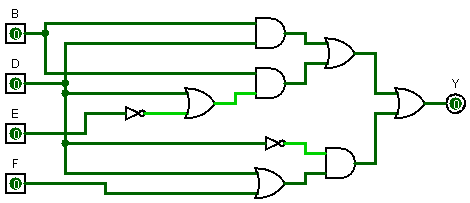
* 1. **W=BC+~BC**

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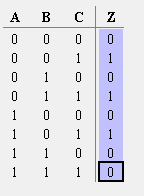
* 1. **X=~AB+~AB~C+~ABCD+~AB~C~DE**

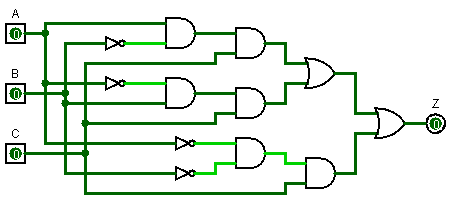
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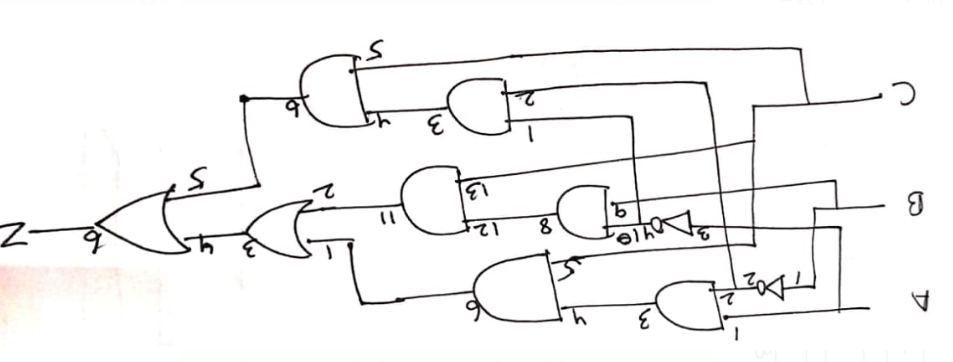
* 1. **Y=BD+B(D+~E)+~D(D+F)**

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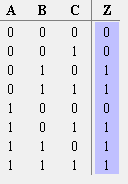
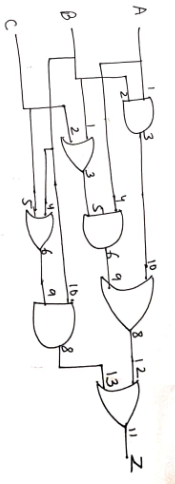
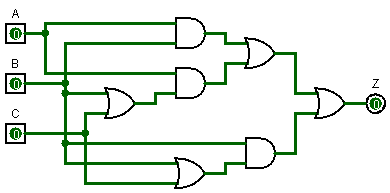
* 1. **Z=A~BC+~ABC+~A~BC**



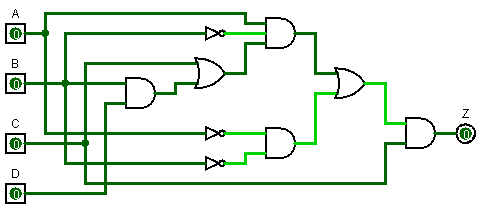
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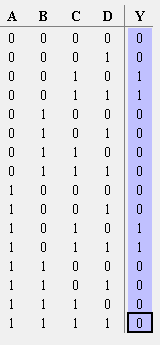


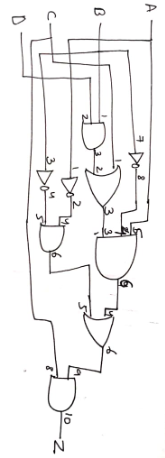
* 1. **AB+A(B+C)+B(B+C)**

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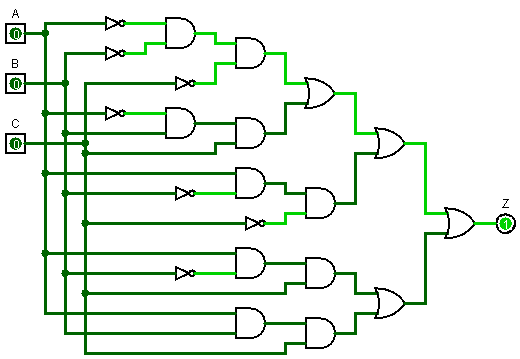
* 1. **(A~B(C+BD)+~A~B)C**

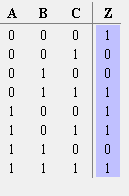
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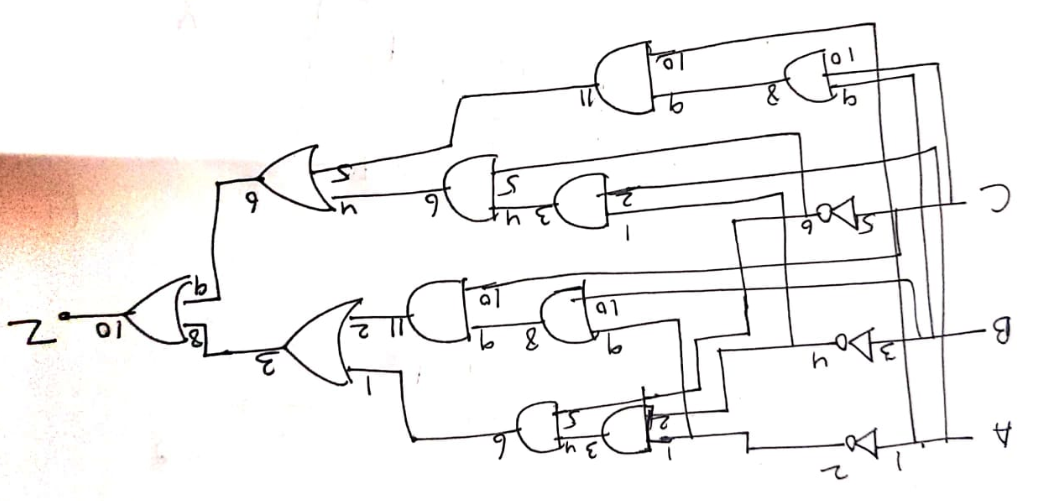




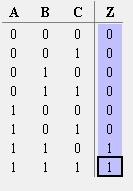
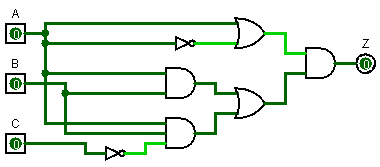
* 1. **~A~B~C+~ABC+A~B~C+A~BC+ABC**

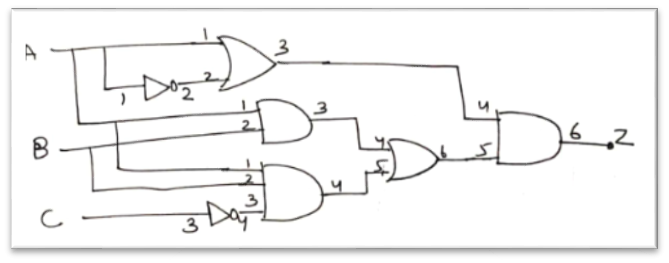
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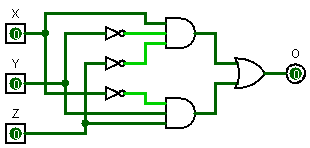
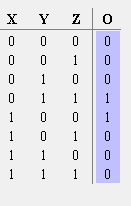


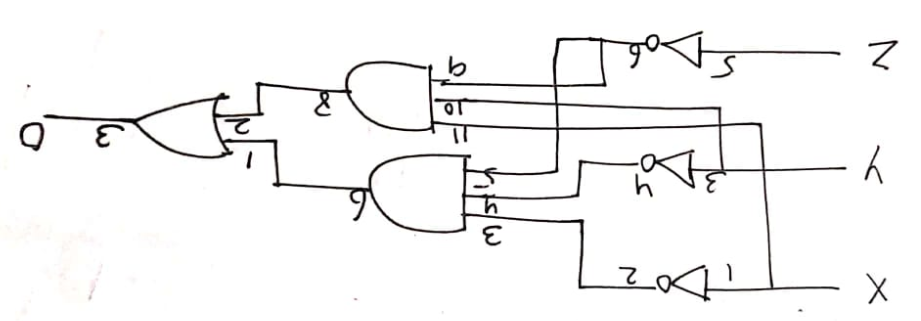
* 1. **(A+~A)(AB+ AB~C)**

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* 1. **X~Y~Z+~XYZ**

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# Laboratory 2

Title of the Laboratory Exercise:

**Build a circuit which is dual of the given expression. Verify using truth table.**

Introduction and Purpose of Experiment

1. Aim and Objectives

Aim

* To Design logic expression and realise the dual

1. Objectives

At the end of this lab, the student will be able to

* Students should be able to realise the expression and its dual

1. Experimental Procedure

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| --- |
| Aim and objective |
| Requirement and equipment used |
| Simulation and realization |
| Verification results and Analysis |
| Conclusion |
| Limitations and Recommendations |
| Viva |

1. Questions

Build a circuit which is dual of the given expression. Verify using truth table.

~(~(AB)~(CD))=AB+CD

~(~(AB)C)=AB+~C

~(A~(BC))=~A+BC

~(ABC)=~A+~B+~C

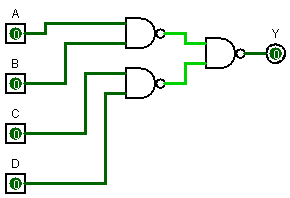
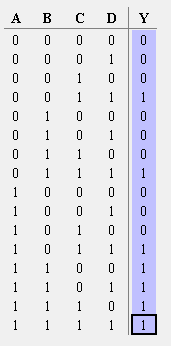
A(~(B+C)=A~B~C

~(~AB(C+~D)+E)=A~E+~B~E+~CD~E

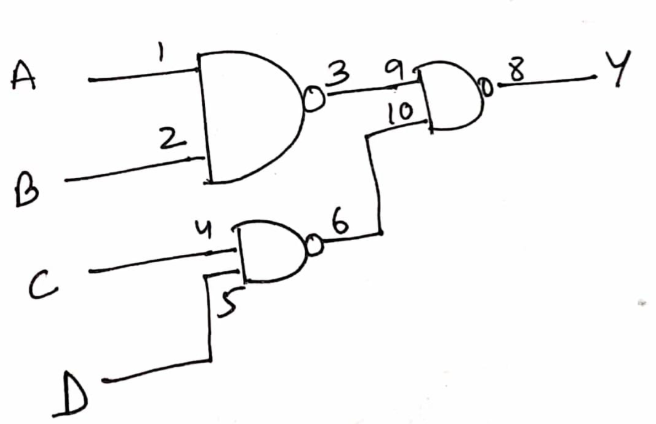
## Solution:

* 1. **~(~(AB)~(CD))=AB+CD**

LHS :

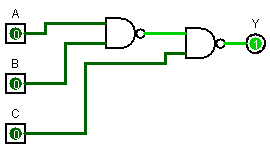
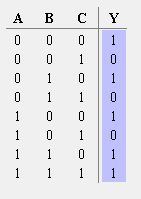


RHS:

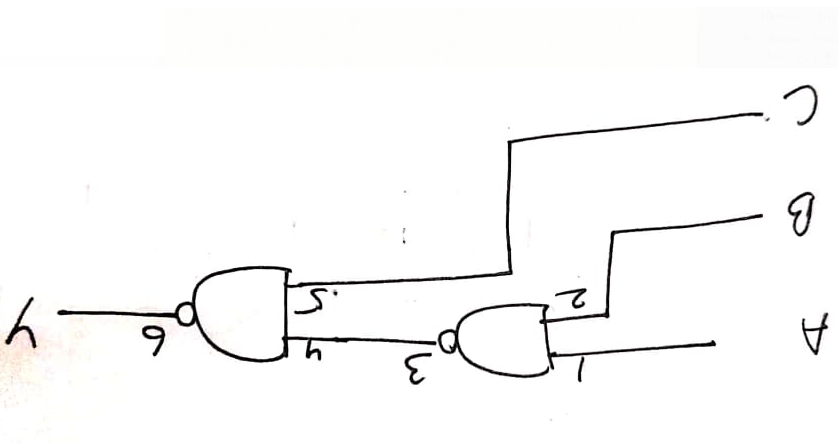


b. **~(~(AB)C)=AB+~C**

LHS:

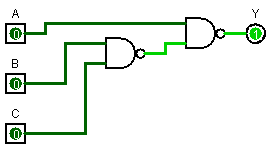
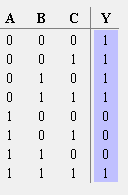


RHS:

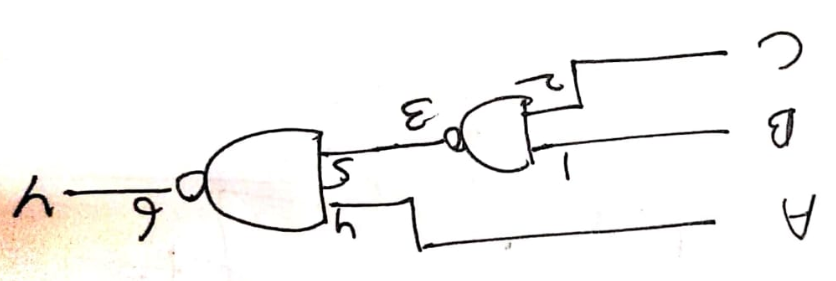


c. **~(A~(BC))=~A+BC**

LHS:

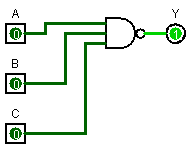
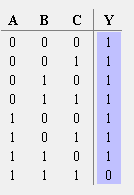
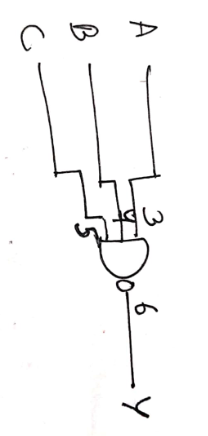


RHS:



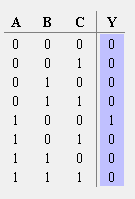
d. **~(ABC)=~A+~B+~C**

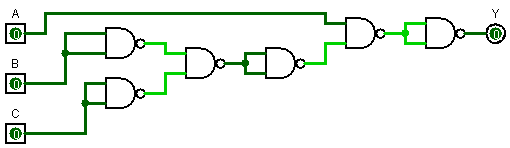
LHS:



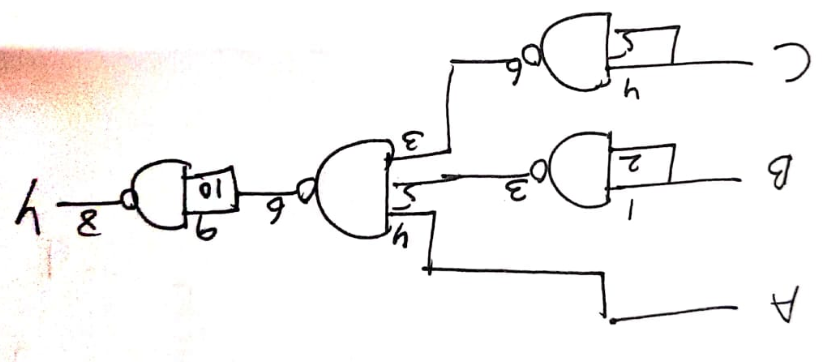
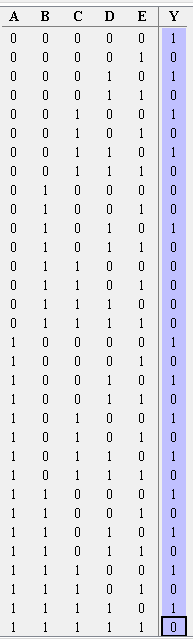
RHS

e. **A(~(B+C))=A~B~C**

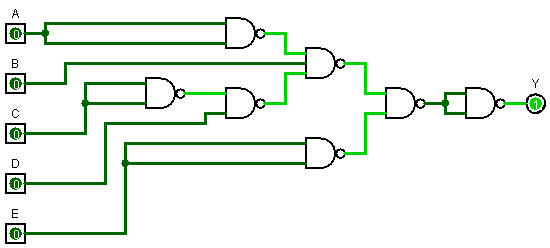
LHS



RHS:



f. **~(~AB(C+~D)+E)=A~E+~B~E+~CD~E**

LHS:

RHS:

